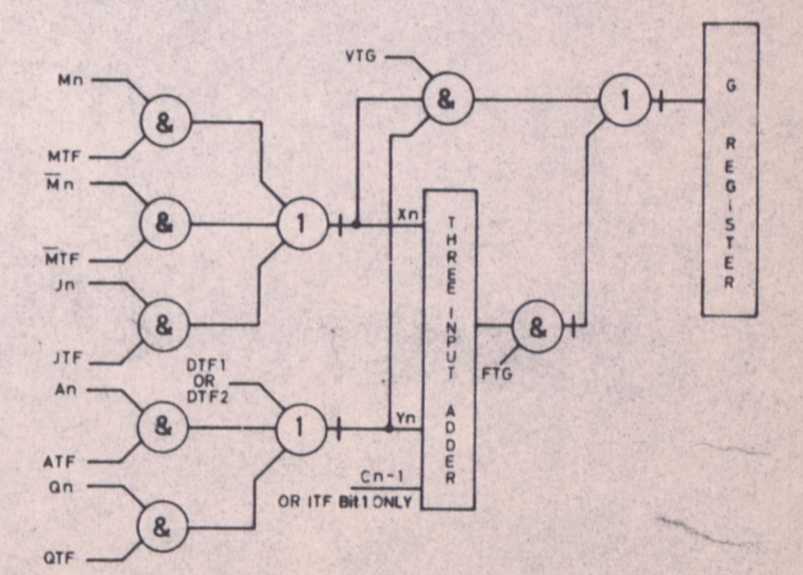


NOTE: TERMS MARKED WITH THE SUFFIX 'm' i.e. VTGm COME DIRECTLY FROM THE MATRIX AND A TRUE OUTPUT IS REPRESENTED BY 0 VOLTS.

THE OUTPUT OF THE ADDER IS EQUAL TO THE SUM OF $x_n + y_n + C_{n-1}$. AS THERE CAN BE NO C_{n-1} TO BIT 1 THE ITF SIGNAL IS TAKEN TO THIS INPUT. HENCE IF ITF OCCURS THEN ONE IS ADDED TO ANY OTHER INPUT TO THE ADDER. DTF1 MAKES y_n ON BITS 1-13 EQUAL TO 1. HENCE IF DTF1 AND VTG OCCUR, THE G REGISTER WILL COPY THE FIRST 13 BITS OF THE REGISTER GATED INTO x_n . DTF1 & DTF2 MAKES y_n ON ALL BOARDS EQUAL TO 1. HENCE IF THIS OCCURS WITH FTG THEN A 'FULLHOUSE' IS ADDED TO x_n , i.e. ONE IS SUBTRACTED.



SYMBOLIC REPRESENTATION OF ADDER.

920B COMPUTER REGISTER MODULE AND CONTROL WAVEFORMS

A19

SHEET 2 OF 2

TO BE READ IN CONJUNCTION WITH 322A.7191

LATEST MI INCORPORATED, MI 2993 3221 2998

ISSUE No.	1	MATERIAL	FINISH	ELLIOTT BROTHERS (LONDON) LTD
ALT. No.	1681	TOLERANCES: DECIMAL: FRACTIONAL: ANGULAR: DIMENSIONS: UNLESS OTHERWISE STATED		TITLE 920B COMPUTER REGISTER MODULE AND CONTROL WAVEFORMS
DATE	7/10/66	DRAWN L. J. EVERETT		
INITIALS	L. J. E.	CHECKED CS794	APPROVED: DATE	SHEET 2
PARTS LIST No.				